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| EXAMINER | |
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| HSU, JONI | |
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| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/901,936 | NOONBURG, DEREK B. | |
| | Examiner | Art Unit | |
| | Joni Hsu | 2628 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/7/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on November 7, 2006 was filed after the mailing date of the application on July 9, 2001. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Response to Amendment*

2. In light of Applicant's amendments to Claims 24 and 25, the 35 U.S.C. 101 rejections have been withdrawn.

3. Applicant's arguments filed November 7, 2006 have been fully considered but they are not persuasive.

4. With regard to Claim 1, Applicant argues that Artieri (US005579052A) does not teach retrieving the data in any other fashion, or selecting a packetization scheme based upon the location in the memory and then combining the data into packets according to that scheme. Rather, Artieri is limited to storing and reading the data in the same packetized form as it is stored, and no other method of retrieving the data is disclosed (page 13).

In reply, the Examiner disagrees. Artieri discloses determining the position in the picture memory from which packets of data must be transferred. The instruction processor includes an

address register containing the address at which a read operation is carried out. After determining the position, the content of the address register is modified. This modification may consist in an incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks) (Col. 16, lines 33-47). Therefore, based on the locations of the read data, the packets can be combined by reading data at successive addresses, or the packets can be combined by a more complex calculation, such as a recursive calculation to extract a picture line from a sequence of macro-blocks. Therefore, Artieri discloses selecting a packetization scheme based upon the location in the memory and then combining the data into packets according to that scheme.

5. With regard to Claim 19, Applicant argues that Artieri fails to show packing the read data into data packets according to the specifications of a read command but rather only shows that a data packet may have a header containing decoding parameters. There is no connection shown between the packetization scheme and the read command (page 14).

In reply, the Examiner disagrees for the same reasons given above.

*Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-6, 14-17, 19-32, and 34-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Artieri (US005579052A).

8. With regard to Claim 1, Artieri discloses a method for generating memory requests to fetch read data from a plurality of locations in a memory (*read instruction, modification may consist in an incrementation (which amounts to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks),* Col. 16, lines 40-47), the memory comprising a plurality of memory pages, each of the memory pages having a plurality of words (*picture memory is a DRAM, DRAM is partitioned into several pages, words of the page*, Col. 18, lines 21-30), the method comprising the steps of determining the locations of the read data in the memory; selecting a packetization scheme based on the locations of the read data; assembling at least one read command for addressing the plurality of locations of the read data; and fetching the read data from the memory locations and combining it into a plurality of data packets in accordance with the selected packetization scheme (*determine the position in the picture memory from which packets of data must be transferred, read instruction, modification may consist in an*

*incrementation (which amounts to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks,* Col. 16, lines 33-47; *provide packet to be processed to the pipeline circuit, receives the compressed data from the memory bus and extracts the packets therefrom*, Col. 3, lines 34-51). Artieri discloses determining the position in the picture memory from which packets of data must be transferred. The instruction processor includes an address register containing the address at which a read operation is carried out. After determining the position, the content of the address register is modified. This modification may consist in an incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks) (Col. 16, lines 33-47). Therefore, based on the locations of the read data, the packets can be combined by reading data at successive addresses, or the packets can be combined by a more complex calculation, such as a recursive calculation to extract a picture line from a sequence of macro-blocks. Therefore, Artieri discloses selecting a packetization scheme based upon the location in the memory and then combining the data into packets according to that scheme.

9. With regard to Claim 2, Artieri discloses the step of sending the at least one read command corresponding to the plurality of data packets to the memory (*determine the position in the picture memory from which packets of data must be transferred, read instruction, modification may consist in an incrementation (which amounts to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a*

*recursive calculation to extract a picture line from a sequence of macro-blocks,* Col. 16, lines 33-47).

10. With regard to Claim 3, Artieri discloses the step of fetching the read data in response to sending the at least one read command (Col. 16, lines 33-47).

11. With regard to Claim 4, Artieri discloses that the read data comprises a reference pixel chunk having a luminance chunk and a chrominance chunk (*macro-block includes a luminance block formed by 4 8x8-pixel blocks and a chrominance block formed by 2 8x8-pixel blocks, predictor macro-block,* Col. 1, lines 30-45).

12. With regard to Claim 5, Artieri discloses that the step of determining the location of the read data further comprises receiving at least a set of motion vectors pointing to the reference pixel chunk (*to find the predictor macro-block MBp, a movement compensation vector defines the position of the MBp*, Col. 1, lines 41-45; *memory controller receiving movement compensation vectors*, Col. 4, lines 24-28).

13. With regard to Claim 6, Artieri discloses the step of determining a first set of components associated with the reference pixel chunk based on the at least a set of motion vectors (Col. 1, lines 26-35; Col. 2, lines 23-44).

14. With regard to Claim 14, Artieri discloses that each of the at least one read command includes specifications for combining selected ones of the plurality of words from selected ones of the plurality of memory pages into the plurality of data packets (*once a page is selected, the words of this page are all accessible, luminance blocks are store in a first page, and the chrominance blocks are stored in another page, separation and grouping of the blocks during transfers of macro-blocks*, Col. 18, lines 21-30; *determine the position in the picture memory from which packets of data must be transferred*, Col. 16, lines 33-47; *provide packet to be processed to the pipeline circuit, receives the compressed data from the memory bus and extracts the packets therefrom,* Col. 3, lines 34-51).

15. With regard to Claim 15, Artieri discloses that the plurality of data packets is equal to or less than a predetermined number (*partitioning the packet into p sub-packets*, Col. 17, lines 45-49; *the size of this packet of data being fixed and, for example, equal to half he size of the FIFO*, Col. 16, lines 6-10).

16. With regard to Claim 16, Artieri discloses the case in which the predetermined number is three (Col. 17, lines 45-62), but this is just an example and the predetermined number can inherently be adjusted to any number, and therefore can be four. Artieri discloses that the selected ones of the plurality of memory pages is two (Col. 18, lines 31-37).

17. With regard to Claim 17, Artieri discloses the case in which the predetermined number is three (Col. 17, lines 45-62), but this is just an example and the predetermined number can

inherently be adjusted to any number, and therefore can be four. Artieri discloses an example in which the selected ones of the plurality of memory pages is two (Col. 18, lines 31-37). However, this is just an example, and Artieri discloses that it is possible to execute a larger number of page changes, and therefore the selected ones of the plurality of memory pages can be adjusted to any number, and therefore can be three.

18. With regard to Claim 19, Artieri discloses a method for packing read data into data packets (Col. 3, lines 34-51), the read data being stored in a plurality of locations in a memory (Col. 16, lines 43-47), the memory comprising a plurality of memory pages (Col. 18, lines 21-30), the method comprising the steps of receiving at least one read command requesting the read data, the at least one read command comprising specifications for including in the data packets a selected portion of the read data from at least one of the plurality of memory pages (Col. 16, lines 32-47; Col. 18, lines 38-52); sending instructions to the memory according to the at least one read command received, the instructions relating to a manner in which the read data requested is to be obtained from the memory; receiving the read data from the memory in response to the memory receiving the instructions; and packing the read data received into the data packets according to the specifications of each of the at least one read commands (Col. 16, lines 32-47; Col. 3, liens 34-51). Artieri discloses determining the position in the picture memory from which packets of data must be transferred. The instruction processor includes an address register containing the address at which a read operation is carried out. After determining the position, the content of the address register is modified. This modification may consist in an incrementation (which amount to write or to read data at successive addresses in the

picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks) (Col. 16, lines 33-47). Therefore, based on the locations of the read data, the packets can be combined by reading data at successive addresses, or the packets can be combined by a more complex calculation, such as a recursive calculation to extract a picture line from a sequence of macro-blocks. Therefore, Artieri discloses packing the read data into data packets according to the specifications of a read command.

19. With regard to Claim 20, Artieri discloses that the read data is a reference pixel chunk comprising a luminance chunk and a chrominance chunk (Col. 1, lines 30-45).

20. With regard to Claim 21, Artieri discloses a method for reassembling reference pixel data from a plurality of data packets into a luminance chunk and a chrominance chunk (Col. 18, lines 21-37; Col. 3, lines 34-51), comprising the steps of receiving the plurality of data packets, each data packet comprising a portion of a reference pixel chunk including the luminance chunk and the chrominance chunk; determining a packetization scheme used to packetize the luminance and chrominance chunks into the plurality of data packets based upon the locations in memory of the data; and unpacking the plurality of data packets into a reassembled luminance chunk and a reassembled chrominance chunk based on the packetization scheme (Col. 1, lines 30-45; Col. 3, lines 34-51). Artieri discloses determining the position in the picture memory from which packets of data must be transferred. The instruction processor includes an address register containing the address at which a read operation is carried out. After determining the position, the content of the address register is modified. This modification may consist in an

incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks) (Col. 16, lines 33-47). Therefore, based on the locations of the read data, the packets can be combined by reading data at successive addresses, or the packets can be combined by a more complex calculation, such as a recursive calculation to extract a picture line from a sequence of macro-blocks. Therefore, Artieri discloses selecting a packetization scheme based upon the location in the memory and then combining the data into packets according to that scheme.

21. With regard to Claim 22, Artieri discloses the steps of forming prediction blocks by arranging the plurality of data packets unpacked with any information related to motion vectors (Col. 1, lines 36-45; Col. 3, lines 34-50), and combining blocks with associated macroblocks to form a reconstructed macroblock (*macro-block is combined with two predictor macro-blocks, these two pictures are respectively former and subsequent pictures, with respect to the currently reconstructed picture*, Col. 1, line 64-Col. 2, line 3).

22. With regard to Claim 23, Artieri discloses the step of writing the reconstructed macroblock to a memory (*store the currently reconstructed picture*, Col. 7, lines 47-50); selecting a packetization scheme based on a location of read data and on fitting the read data into the plurality of data packets; and assembling at least one read command for fetching the read data from the memory in accordance with the packetization scheme selected (Col. 16, lines 32-47).

23. With regard to Claims 24 and 26, Claims 24 and 26 are similar in scope to Claim 1, and therefore is rejected under the same rationale.

24. With regard to Claims 25 and 27, Claims 25 and 27 are similar in scope to Claim 19, and therefore is rejected under the same rationale.

25. With regard to Claim 28, Artieri discloses a system for decoding pictures in a compressed video bit stream (*picture decompression system*, Col. 3, lines 6-8; *MPEG decoder*, Col. 6, lines 33-34), comprising a memory (15, Figure 3; Col. 6, lines 37-41) having a plurality of memory pages (Col. 18, lines 21-30) storing reference pixel data (Col. 7, lines 52-67); an address generator (24) coupled to the memory for generating memory commands for fetching the reference pixel data from the memory; means for packing the fetched reference pixel data into a plurality of data packets according to the specifications of the memory commands (*determine the position in the picture memory from which packets of data must be transferred, instruction processor includes an address register containing the address at which a transfer operation is carried out, instructions to adequately modify the content of the address register, this adequate modification may consist in an incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks),* Col. 16, lines 32-47; *memory controller 24 includes instruction processing unit 50*, Col. 13, lines 18-25); a reference data assembly module (FIFOs) coupled to the address generator for receiving from the

memory the plurality of data packets (*exchanges on the MBUS are controlled by a memory controller 24 that serves to carry out, transfer operations between these FIFOs and the picture memory*, Col. 6, lines 45-48); and means for unpacking the plurality of data packets and resassembling the fetched reference pixel data into a reassembled video bit stream (*macro-block is reconstructed by using a predictor macro-block fetched in a previously decoded picture*, Col. 1, lines 36-45; *receives the compressed data from the memory bus and extracts the packets therefrom*, Col. 3, lines 34-50). Artieri discloses determining the position in the picture memory from which packets of data must be transferred. The instruction processor includes an address register containing the address at which a read operation is carried out. After determining the position, the content of the address register is modified. This modification may consist in an incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks) (Col. 16, lines 33-47). Therefore, based on the locations of the read data, the packets can be combined by reading data at successive addresses, or the packets can be combined by a more complex calculation, such as a recursive calculation to extract a picture line from a sequence of macro-blocks. Therefore, Artieri discloses packing the fetched reference pixel data into a plurality of data packets according to the specifications of the memory commands.

26. With regard to Claim 29, Artieri discloses that the reference pixel data comprises a luminance chunk and a chrominance chunk (Col. 1, lines 30-45).

27. With regard to Claim 30, Artieri discloses that the memory commands comprises specification for combining selected portions of the reference pixel data from a selected one or more of the plurality of memory pages into at least one of the plurality of data packets (Col. 16, lines 32-47).

28. With regard to Claim 31, Artieri discloses that the reference data assembly module (FIFO) unpacks the plurality of data packets to transform the reference pixel data into a reassembled luminance chunk and a reassembled chrominance chunk (*the luminance block is stored in a first page and the chrominance block is stored in another page*, Col. 18, lines 31-37; *memory controller 24 then transfers the compressed data from memory 15 to the FIFO 21, in the order they were written*, Col. 10, lines 16-18).

29. With regard to Claim 32, Artieri discloses that the reference data assembly module comprises a plurality of data buffers, each data buffer being configured to receive one of the plurality of data packets (*the size of the FIFOs is two packets of data, one packet of data corresponding to a macro-block fraction*, Col. 9, lines 45-48).

30. With regard to Claim 34, Artieri discloses that the reference data assembly module comprises a plurality of data buffers for buffering a reassembled luminance chunk and a reassembled chrominance chunk (Col. 18, lines 31-37; Col. 10, lines 16-18).

31. With regard to Claim 35, Artieri discloses a variable length decoding module (10, Figure 3) configured to extract a set of motion vectors corresponding to a macroblock in the compressed video bit stream (*movement compensation vectors, these decoding parameters are decoded by the VLD circuit itself to decode the vectors and data of the macro-blocks,* Col. 7, lines 10-15; *MPEG decoder, couples the compressed data input bus to the input of the variable length decoder (VLD) 10*, Col. 6, lines 33-39).

32. With regard to Claim 36, Artieri discloses that the variable length decoding module (10, Figure 3) sends the extracted set of motion vectors to the address generator (24) (Col. 7, lines 10-15).

33. With regard to Claim 37, Artieri discloses a memory interface unit (instruction register) coupled to the memory (*instruction register is coupled to the output of ROM 54, an instruction is executed substantially as soon as it is loaded in the instruction processor 50,* Col. 13, lines 59-64).

34. With regard to Claim 38, Artieri discloses that the memory interface unit further comprises a memory queue for storing the generated memory commands from the address generator (Col. 13, lines 59-64).

35. With regard to Claim 39, Artieri discloses that at least one of the plurality of data packets includes the reference pixel data from at least two of the plurality of memory pages (Col. 18,

lines 31-37) based on the generated memory commands in the memory queue (Col. 16, lines 32-47; Col. 13, lines 59-64).

36. With regard to Claim 40, Artieri discloses that the memory interface unit (24, Figure 5; Col. 13, lines 18-25) further comprises a sequencer for forwarding the generated memory commands to the memory to obtain the reference pixel data based on specifications (*the beginning of a transfer program of a packet of data includes an instruction that writes in this address register the content of the data pointer,* Col. 16, lines 32-47).

37. With regard to Claim 41, Artieri discloses that the memory interface unit (24) further comprises a packet assembly unit (FIFO) for assembling the plurality of data packets of the reference pixel data obtained from the memory (Col. 6, lines 45-51; Col. 9, lines 45-52).

38. Thus, it reasonably appears that Artieri describes or discloses every element of Claims 1-6, 14-17, 19-32, and 34-41 and therefore anticipates the claims subject.

***Claim Rejections - 35 USC § 103***

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

41. Claims 7, 9, 10, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Artieri (US005579052A) in view of McGuinness (US006104416A).

42. With regard to Claim 7, Artieri is relied upon for the teachings as discussed above relative to Claim 4.

However, Artieri does not teach that the step of selecting a packetization scheme further comprises combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages. However, McGuinness discloses combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages (Col. 8, lines 51-67; *luminance Y and both chrominance Cr and Cb are stored in one 32 byte word*, Col. 10, lines 19-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Artieri so that the step of selecting a packetization scheme

further comprises combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages as suggested by McGuinness because McGuinness suggests that if the luminance chunk overlaps more than one of plurality of memory pages, then the accessing would take a long time (Col. 8, lines 51-67), and therefore combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of data packets to be sent from the memory allows all of the components to be retrieved in one word, reducing latency during rasterization without increasing the time needed to retrieve pixel for decoding because all of the components for one tile can sill be retrieved in one burst (Col. 10, lines 19-30).

43. With regard to Claim 9, Artieri does not teach that the step of selecting a packetization scheme further comprises combining a first part of the chrominance chunk and a second part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the chrominance chunk overlaps more than one of the plurality of memory pages. However, McGuinness discloses combining a first part of the chrominance chunk and a second part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the chrominance chunk overlaps more than one of the plurality of memory pages (Col. 8, lines 51-67; *both chrominance components are stored in one word*, Col. 9, lines 55-65). This would be obvious for the same reasons given in the rejection for Claim 7.

44. With regard to Claim 10, Artieri does not teach the step of placing a virtual memory page boundary across the luminance chunk, the virtual memory page boundary being associated with the packetization scheme. According to the disclosure of this application, a virtual page boundary is placed to split the left 2 words of each row. Therefore, the chunk is still considered as falling across four pages A-D. However, pages B and D are actually part of pages A and C [0069-0070]. This is done to create a symmetry that allows the reduction of the number of cases that need to be considered for packetization [0068]. McGuinness describes interlacing the luminance Y and both chrominance Cr and Cb so that all of the components can be retrieved in one word, reducing latency during rasterization without increasing the time needed to retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (Col. 10, lines 26-30). Storing the chrominance components so interlaced enables the FIFO that stores the chrominance to have the same structure as the FIFO storing the luminance (Col. 10, lines 8-9), and therefore creates symmetry. Therefore, McGuinness discloses the step of placing a virtual memory page boundary across the luminance chunk, the virtual memory page boundary being associated with the packetization scheme.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Artieri to include the step of placing a virtual memory page boundary across the luminance chunk, the virtual memory page boundary being associated with the packetization scheme as suggest by McGuinness because MGuinness suggests the advantage of reducing latency (Col. 9, line 60-Col. 10, line 9).

45. With regard to Claim 11, Artieri does not teach the step of placing a virtual memory page boundary across the chrominance chunk, the virtual memory page boundary being associated with the packetization scheme. According to the disclosure of this application, a virtual page boundary is placed to split the left 2 words of each row. Therefore, the chunk is still considered as falling across four pages A-D. However, pages B and D are actually part of pages A and C [0069-0070]. This is done to create a symmetry that allows the reduction of the number of cases that need to be considered for packetization [0068]. McGuinness describes interlacing the luminance Y and both chrominance Cr and Cb so that all of the components can be retrieved in one word, reducing latency during rasterization without increasing the time needed to retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (Col. 10, lines 26-30). Storing the chrominance components so interlaced enables the FIFO that stores the chrominance to have the same structure as the FIFO storing the luminance (Col. 10, lines 8-9), and therefore creates symmetry. Therefore, McGuinness discloses the step of placing a virtual memory page boundary across the chrominance chunk, the virtual memory page boundary being associated with the packetization scheme. This would be obvious for the same reasons given in the rejection for Claim 10.

46. With regard to Claim 18, Artieri does not specifically teach that the plurality of data packets comprise 16 words. However, McGuinness describes that the plurality of data packets comprise 16 words (Col. 9, lines 7-11).

It would have been obvious to one of ordinary skill in the art to modify the device of Artieri so that the plurality of data packets comprise 16 words as suggested by McGuinness because McGuinness suggests that this is a common size for a data packet (Col. 9, lines 7-11).

47. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Artieri (US005579052A) in view of Sorin (US006631164B1).

Artieri is relied upon for the teachings as discussed above relative to Claim 4.

However, Artieri does not teach that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages. However, Sorin discloses accessing blocks by combining them in a certain manner (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39), and therefore the blocks are to be combined in a data packet in a certain manner. Therefore, Sorin describes that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Artieri so that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the

luminance chunk overlaps more than one of the plurality of memory pages as suggested by Sorin because Sorin suggests that typically, motion estimation calculations are performed on the luminance values alone (Col. 1, lines 46-61).

48. Claims 12, 13, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Artieri (US005579052A) in view of Levy (US005170251A).

49. With regard to Claim 12, Artieri is relied upon for the teachings as discussed above relative to Claim 1. Artieri describes that the packetization scheme selected maps a first set of components to a second set of components (Col. 16, lines 32-47; Col. 18, lines 31-52).

However, Artieri does not teach selecting the packetization scheme by a table lookup. However, Levy describes selecting the packetization scheme by a table lookup (Col. 2, lines 20-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Artieri to include selecting the packetization scheme by a table lookup as suggested by Levy. The speed gained by using a lookup table can be significant, since retrieving a value from memory is often faster than undergoing an expensive computation. Lookup tables are well-known in the art, widely used, and can be found in many publications, such as the Wikipedia Encyclopedia.

50. With regard to Claim 13, Artieri discloses that the first set of components comprises the read data corresponding to the luminance chunk and the chrominance chunk, and the second set of components comprises the selected ones of the plurality of words (Col. 18, lines 21-37).

51. With regard to Claim 33, Artieri discloses that the reference data assembly module comprises an additional module (14, Figure 3) for reassembling the reference pixel data based on a set of motion vectors (*once it has received the macro-block type and the vectors, the filter 14 is ready to receive a predictor macro-block*, Col. 10, lines 32-34; *filter 14 includes two FIFOs; one FIFO is intended to receive forward macro-block; the other FIFO is intended to receive backward macro-blocks*, Col. 10, lines 52-65; *macro-block is reconstructed by using a predictor macro-block, movement compensation vector that defines the position of the predictor macro-block*, Col. 1, lines 39-45) and packetization scheme used to form the plurality of data packets (*FIFO of filter 14*, Col. 11, lines 26-34; *size of the FIFOs is two packets of data*, Col. 9, lines 45-52).

However, Artieri does not teach a table lookup used to form the plurality of data packets. However, Levy describes a table lookup used to form the plurality of data packets (Col. 2, lines 20-30), as discussed in the rejection for Claim 12.

***Prior Art of Record***

"Lookup table." http://en.wikipedia.org/wiki/Lookup_table.

*Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER